



RM-7739

B. E. IV (Sem. VIII) (ECC) Examination

May / June - 2010

Advance Microprocessor
Elective - I

Time : 3 Hours]

[Total Marks : 100

Instructions :

(1)

નીચે દર્શાવેલ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી. Fillup strictly the details of signs on your answer book.	Seat No. :
Name of the Examination :	<input type="text"/>
<input type="text" value="B. E. 4 (Sem. 8) (ECC)"/>	<input type="text"/>
Name of the Subject :	<input type="text"/>
<input type="text" value="Advance Microprocessor : Elective - 1"/>	<input type="text"/>
Subject Code No. : <input type="text" value="7"/> <input type="text" value="7"/> <input type="text" value="3"/> <input type="text" value="9"/>	<input type="text"/>
Section No. (1, 2,.....) : <input type="text" value="1&2"/>	<input type="text"/>
	Student's Signature

- (2) Attempt **all** questions.
- (3) Figures to the **right** indicate full marks.
- (4) Assume suitable data wherever **necessary** and mention clearly your assumptions.
- (5) Use of non programmable scientific calculators is allowed.

Section-I

Q.1(A) Answer the followings: **10**

- (i) What is function of QS0 and QS1 pins of 8086 in maximum mode.
- (ii) The 8087 internally stores all data in which format? Why?
- (iii) Explain function of busy and acknowledge pins in centronics parallel printer interface.
- (iv) State function of single transfer mode in DMA controller 8237.
- (v) State voltage levels of RS 232.

(B) Write a program to find the resonant frequency of an LC tuned circuit using 8087 and 8086 instructions and directives. **05**

(C) Explain the internal architecture of 8087. **05**

Q.2 (A) What do you mean by closely coupled and loosely coupled systems? Explain the working of closely coupled systems. **07**

(B) Explain in detail functions of PCI and VESA bus. **08**

OR

(A) Why DRAM requires refreshing? Explain in brief the characteristics of refreshing DRAM. **07**

(B) Draw the timing diagram of handshake signals in case of centronics parallel interface of printer. Explain the use of all handshake signals and logic to achieve data transfer between PC and printer. **08**

Q.3 Attempt any three:

15

- (A) Draw and explain timing for maximum mode bus requests and grants.
- (B) Compare RS 232, RS 423 and RS 449 serial standards.
- (C) Explain 6845 CRT monitor interface.
- (D) Explain the daisy chaining priority scheme in loosely coupled system.
- (E) Explain interrupt sequence in 8086 system when 8259 is connected to it.

Section-II

Q.4(A) Answer the followings:

10

- (i) The Pentium can execute _____ instructions simultaneously.
- (ii) When 80386 operated in protected mode memory segment size range from _____ to _____.
- (iii) Using _____ the Pentium Pro is able to look ahead as many as 30 instructions.
- (iv) At any given time the 80386 has _____ active segments.
- (v) The 386 keeps track of the 32 most recently used page frames in the _____.
- (vi) Using 386 debug registers _____ different breakpoint addresses can be set.
- (vii) The P6 processors can execute _____ instructions per cycle.
- (viii) For a memory interface to work properly, the access time provided by the processor must be _____ the access time of the memory chip.
- (ix) INT _____ is useful for mouse operations.
- (x) To determine if a memory location is stored in the cache the _____ bits are compared with the high order memory address bits.

(B) Which of the following 80X86 microprocessors have 16 bit internal data bus?
a. 8086 b. 8088 c. 80286 d. 80386SX e. 80386 f. 80486DX g. Pentium h. 80186 **04**

(C) Explain why and how the following microprocessor features affect the processing rate of the chip: (a) clock frequency (b) data bus width (c) internal cache memory **06**

Q.5(A) With the help of functional block diagram explain the various blocks of 80486 processor and their functions in brief. **08**

(B) What do you mean by RISC and CISC architectures? Justify that Pentium uses both RISC and CISC features. **07**

OR

(A) Explain the advantage of having on chip cache memory and cache organization of 80486 cache. **08**

(B) What is Branch prediction and why it is required in pipelined architecture? Explain the Branch prediction in Pentium processor. **07**

Q.6 Attempt any three:

15

- (A) Explain the procedure of assembly language program using assembler tool with the help of flow chart.
- (B) Explain the operations performed by following instructions.
 - (i) MOVSX (ii) XADD (iii) BSWAP

(C) Write a far procedure 'read2' to read a character from keyboard and reserve locations for storage of read data. The main program uses this procedure to call it 10 times and store the data as a string of characters in memory reserved by procedure. Use FAR, PUBLIC and EXTERN directives.

(D) Calculate the data transfer rate for an 8088 processor running at 4.77MHz. Compare this result to a Pentium processor with 66MHz bus frequency.

(E) Explain five stages of pipeline in 80486. How it results in reduced instruction cycle times?
